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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,335	09/19/2006	Simon Deleonibus	129343	9898

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EXAMINER	
HUBER, ROBERT T	
ART UNIT	PAPER NUMBER
2892	
MAIL DATE	DELIVERY MODE
11/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,335	DELEONIBUS, SIMON	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in France on March 25, 2004. It is noted, however, that applicant has not filed a certified copy of the 0403073 application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Sorada et al. (US 7,119,417 B2).

a. Regarding claim 1, **Sorada discloses a method for making a field effect transistor** (e.g. figures 12 – 14, disclosed in col. 10, lines 29 - 34 and 43 - 59 to be a second embodiment similar to the first embodiment shown in figures 1 - 10, except with different formations of the source, drain, and gate regions) **comprising a source and a drain** (e.g. figure 14, source and drains regions 110 and 301) **connected by a channel** (channel 105) **controlled by a gate electrode** (gate electrode 107) **separated from the channel by a gate**

insulator (gate insulator 106), **the channel being formed in a diamond-like carbon layer** (layer 103, disclosed in col. 10, lines 24 - 25 to be silicon-germanium-carbon, and therefore may be considered to be a diamond-like carbon layer), **the method successively comprising**

- deposition of said diamond-like carbon layer on a substrate (as seen in figure 3, diamond-like carbon layers 103 is deposited on substrate 101),

- deposition of an insulating gate layer on the diamond-like carbon layer (as seen in figure 4, insulating gate layer 106 is deposited on carbon layer 103),

- deposition, on the insulating gate layer, of at least one conducting layer and etching of the latter so as to form the gate electrode (e.g. as seen in figure 5 and disclosed in col. 7, lines 50 – 55, conducting layer 107 is formed on the gate insulation layer 106 and then etched),

- **deposition of an insulating material on flanks of the gate electrode to form a lateral insulator** (as seen in figure 7, insulation material 109'),

- etching of the gate insulating layer (as seen in figure 9, and disclosed in col. 8, lines 5 – 7),

- etching of the diamond-like carbon layer so as to delineate the channel, in said diamond-like carbon layer (e.g. as seen in figure 9 and disclosed in col. 8, lines 5 – 8, diamond-like carbon layer 103 (disclosed in col. 10, lines 24 – 27) is etched to form the channel region),

- deposition, on each side of the channel, of a semi-conducting material desired to form the source and of a semi-conducting material designed to form the drain (as seen in figure 13, semi-conducting material 301 is formed on each side of the channel to form source and drain regions, as disclosed in col. 10, line 63 - col. 11, line 12).

b. Regarding claim 4, **Sorada discloses the field effect transistor comprising a channel formed by a diamond-like carbon layer** (e.g. transistor as seen in figure 12, with diamond-like carbon layer 103, disclosed in col. 10, lines 24 – 27), **transistor obtained by a method according to claim 1** (e.g. as seen in figures 1 – 10 and 12 – 14, as discussed with respect to claim 1).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sorada in view of Deleonibus (US 6,091,076).

a. Regarding claim 2, **Sorada discloses the method according to claim 1, as cited above, but is silent with respect to the etching of the diamond-like**

carbon layer is isotropic so as to obtain a retraction of the diamond-like carbon layer under the gate insulating layer.

Deleonibus discloses a method of forming a field effect transistor (e.g. figure 10, disclosed in col. 8, line 48) **wherein the etching of the channel layer is isotropic to obtain a retraction (recess) of the channel layer** (retractions 110 and 112, disclosed in col. 8, line 60 – col. 9, line 2) **under the gate insulating layer** (gate insulation layer 52).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the method of Sorada to include a process of an isotropic etching of the channel to form a retraction under the gate insulating layer since Deleonibus discloses a similar method wherein the channel is etched in such a manner to provide a retraction under the gate insulation layer. The combination of the method of Deleonibus for etching the channel with the method of Sorada of a channel formed by a diamond-like carbon layer would yield a process wherein the diamond-like carbon layer channel is formed by an isotropic etch such that it has a retraction under the gate insulating layer . One would have been motivated to form the channel layer with an isotropic etch in order to have a retraction of the channel layer under the gate insulation layer in order to provide an overlap of the gate electrode with the drain and source regions, thereby allowing for more efficient device operation.

b. Regarding claim 3, **Sorada in view of Deleonibus further disclose the method according to claim 2, as cited above, comprising anisotropic etching of the semi-conducting materials in the zones of the substrate not covered by the gate electrode and the lateral insulator** (as disclosed by Sorada in col. 8, lines 1 – 4).

6. Claims 5 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sorada in view of Dennard et al. (US 4,090,289).

a. Regarding claims 5 and 6, **Sorada discloses a transistor according to claim 4, as cited above, but does not explicitly disclose that the channel comprises N- or P- type dopants. However, Sorada discloses that the transistor, as cited with respect to claim 4, may be formed as N- or P- type by variation of the impurities, and used in a CMOS configuration** (col. 10, lines 6 – 14).

Dennard discloses a transistor comprising P-type dopants in the channel, which forms an NMOS (col. 5, lines 52-63), **and that the reverse type (i.e. N-type) may be used to form PMOS transistors** (col. 5, lines 60 - 66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Sorada in order to form PMOS and NMOS transistors with corresponding N-type and P-type dopants in the channel since Sorada discloses that the transistor may be doped with impurities to form

CMOS with n-channel and p-channel transistors, and Dennard explicitly discloses the channels to be doped with N-type or P-type impurities. One would be motivated to dope the channel with impurities since this will directly impact the conductivity of the device, allowing for NMOS or PMOS formation, and subsequent CMOS devices.

b. Regarding claims 7 and 8, **Sorada in view of Dennard further disclose CMOS logic gate, comprising the PMOS and NMOS transistors according to claims 5 and 6, as cited above respectively** (e.g. Sorada discloses the transistors to be used in a CMOS configuration in col. 10, lines 10 - 14. It is well-known in the art that the most fundamental CMOS configuration is an inverter, which is a logic gate), **wherein the PMOS and NMOS type transistors have substantially the same dimensions** (e.g. Sorada discloses in col. 10, lines 6 - 14 disclose forming variations of the p-channel and n-channel transistors by simply changing dopant impurities, and forming the transistors at the same time to form a CMOS device. Therefore a prima facie case of obviousness is established that the transistors are substantially the same size).

Response to Arguments

7. Applicant's arguments with respect to claims 1 - 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
October 30, 2008